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# TRANSMITTAL FORM

*(to be used for all correspondence after initial filing)*

Total Number of Pages in This Submission: 36

| | |
|---|---|
| Application Number | 09/918,600 |
| Filing Date | 7/30/01 |
| First Named Inventor | Tseng |
| Art Unit | 2128 |
| Examiner Name | Saxena, Akash |
| Attorney Docket Number | CAD5048AP07 (16503-302501) |

**ENCLOSURES** *(check all that apply)*

- ☒ Fee Transmittal Form
- ☒ Fee Attached
- ☐ Amendment / Reply
- ☐ After Final
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
- ☐ Reply to Missing Parts under 37 CFR1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) ____
- ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) *(please identify below)*:

Remarks

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

| | | | |
|---|---|---|---|
| Firm | Moser IP Law Group | | |
| Signature | | | |
| Printed Name | Raymond R. Moser Jr. | | |
| Date | May 17, 2006 | Reg. No. | 34,682 |

**CERTIFICATE OF TRANSMISSION/MAILING**

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| Signature | | | |
| Typed or printed name | Kathleen Faughnan | Date | May 17, 2006 |

PTO/SB/17 (12-04v2)
Approved for use through 07/31/2006. OMB 0651-0032
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*Effective on 12/08/2004.*
*Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).*

# FEE TRANSMITTAL for FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

**TOTAL AMOUNT OF PAYMENT** ($) 500.00

| *Complete if Known* | |
|---|---|
| Application Number | 09/918,600 |
| Filing Date | 7/30/01 |
| First Named Inventor | Tseng |
| Examiner Name | Saxena, Akash |
| Art Unit | 2128 |
| Attorney Docket No. | CAD5048AP07 (16503-302501) |

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☒ Deposit Account Deposit Account Number: 50-3582 Deposit Account Name: Moser IP Law Group

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

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**FEE CALCULATION**

**1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

| | FILING FEES | | SEARCH FEES | | EXAMINATION FEES | | |
|---|---|---|---|---|---|---|---|
| | | Small Entity | | Small Entity | | Small Entity | |
| Application Type | Fee ($) | Fee($) | Fee($) | Fee($) | Fee($) | Fee($) | Fees Paid ($) |
| Utility | 300 | 150 | 500 | 250 | 200 | 100 | |
| Design | 200 | 100 | 100 | 50 | 130 | 65 | |
| Plant | 200 | 100 | 300 | 150 | 160 | 80 | |
| Reissue | 300 | 150 | 500 | 250 | 600 | 300 | |
| Provisional | 200 | 100 | 0 | 0 | 0 | 0 | |

**2. EXCESS CLAIM FEES**

| Fee Description | Fee ($) | Small Entity Fee ($) |
|---|---|---|
| Each claim over 20 (including Reissues) | 50 | 25 |
| Each independent claim over 3 (including Reissues) | 200 | 100 |
| Multiple dependent claims | 360 | 180 |

| Total Claims | Extra Claims | Fee($) | Fee Paid ($) |
|---|---|---|---|
| ____ -20 or HP= | ____ | x ____ | = ____ |

HP = highest number of total claims paid for, if greater than 20.

| Indep. Claims | Extra Claims | Fee($) | Fee Paid ($) |
|---|---|---|---|
| ____ - 3 or HP= | ____ | x ____ | = ____ |

HP = highest number of independent claims paid for, if greater than 3.

| Multiple Dependent Claims | |
|---|---|
| Fee ($) | Fee Paid ($) |
| ____ | ____ |

**3. APPLICATION SIZE FEE**

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

| Total Sheets | Extra Sheets | Number of each additional 50 or fraction thereof | Fee ($) | Fee Paid ($) |
|---|---|---|---|---|
| ____ - 100 = | ____ | / 50 = ____ (round up to a whole number) x | | = ____ |

**4. OTHER FEE(S)**

| | Fees Paid ($) |
|---|---|
| Non-English Specification, $130 fee (no small entity discount) | |
| Other (e.g., late filing surcharge): Appeal Brief | $500. |

**SUBMITTED BY**

| | | | | | |
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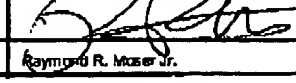
| Signature |  | Registration No. (Attorney/Agent) | 34,682 | Telephone | (732) 935-7100 |
| Name (Print/Type) | Raymond R. Moser Jr. | | | Date | May 17, 2006 |

PATENT
Atty.Dkt. No. CAD5048AP07

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of: Tseng et al.

Serial No.: 09/918,600

Confirmation No.: 8219

Filed: July 30, 2001

For: BEHAVIOR PROCESSOR SYSTEM AND METHOD

§
§
§ Group Art Unit: 2128
§
§ Examiner: Akash Saxena
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§
§
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§

MAIL STOP APPEAL BRIEF - PATENTS
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5/17/06 Katalin Tseng
Date Signature

Dear Sir:

## APPEAL BRIEF

Appellants submit this Appeal Brief to the Board of Patent Appeals and Interferences pursuant to the Notice of Appeal filed on March 9, 2006 in the above-identified application. Please charge the fee of $500.00 (large entity) for filing this brief. The Commissioner is hereby authorized to charge counsel's Deposit Account No. 50-3562 for any fees, including extension of time fees or excess claim fees, required to make this response timely and acceptable to the Office.

05/18/2006 KBETEMA1 00000008 503562 09918600
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## Table of Contents

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## REAL PARTY IN INTEREST

The real party in interest is Verisity Design, Inc. located in San Jose, California.

## RELATED APPEALS AND INTERFERENCES

No other appeals or interferences that are directly affected by, or have a bearing on the Board's decision in the pending Appeal are known to Appellants, Appellants' legal counsel, or the Assignee.

## STATUS OF CLAIMS

Claims 1-37 are pending in the application. Claims 1-37 were finally rejected in the Final Office Action mailed December 9, 2005, as discussed in detail below. The rejection of claims 1-37 and the objection to claims 29 and 34 are presently appealed. The pending claims are shown in the attached Appendix.

## STATUS OF AMENDMENTS

No Amendments to the claims were submitted in this application subsequent to final rejection.

## SUMMARY OF CLAIMED SUBJECT MATTER

A novel Behavior Processor provides a unique architecture for implementing behavior applications, such as monitors, triggers, and memory server that is used in integrated circuit design verification. One embodiment of the present invention comprises a Behavior Processor that is integrated with a reconfigurable computing (RCC) system (i.e., a host workstation containing a software model of at least a portion of the system design that is being emulated) and an RCC hardware array (i.e., an emulator containing the register transfer level (RTL) hardware model). With this configuration, behavioral aspects of a user's integrated circuit design and debug session are implemented in hardware to accelerate the design verification process. Whenever certain conditions are

satisfied as programmed into the Behavior Processor, a callback trigger signal is generated and delivered to the workstation to alert the user and software model. In the past, all behavior functions were implemented in software, resulting in a major bottleneck in the design verification process.

The present invention is a behavior processor system comprising a reprogrammable logic element (e.g., a field programmable gate array (FPGA)) for modeling a hardware model of a portion of a user design that includes a behavior level function (i.e., performed by a behavior processor). Additionally, the behavior processor system comprises a testbench call back process that responds to the behavior level function by sending a signal to a host test bench process. As such, when needed (i.e., upon conditions occurring) the hardware model "calls" a host testbench process (i.e., a software model) to perform certain tasks on an interrupt basis. Thus, behavior functions are performed within the hardware model unless the host testbench process is required.

As suggested in MPEP 1205.02, the Appellant now reads the broadest appealed claims on the specification and on the drawings. For the convenience of the Board of Patent Appeals and Interferences, Appellant's claim 1 (one of the broadest independent claims) is presented below in claim format with elements read on FIGs. 1, 99, and 100 of the drawings. It should be understood, however, that the appealed claims may read on other portions of the specification or other figures that are not listed below.

Independent claim 1 recites (with reference numerals added)::

> A behavior processor system (3100, 3103) for operating a portion (20) of a user design (40) and interfacing with a host testbench process (3101), comprising:
>
> a reprogrammable logic element (3109) for modeling a hardware model of the portion of the user design that includes a behavior level function (3109a); and
>
> a testbench call back process (3109b) for responding to the behavior level function (3109a) in the reprogrammable logic element (3109) by sending a signal to the host testbench process (3101).

The behavior processor (3109) provides a hardware-based "interrupt" -like control. When some condition (as defined by the user based on the user's design) is satisfied within the

behavior processor (3109), the behavior processor sends a control signal (testbench call back) to the RCC system (3107) and any testbench processes (3101). To provide I/O services and system controls during hardware emulation mode, one embodiment of the present invention includes a call testbench primitive, axis _ tbcall, that lets the user use a hardware signal to call a software task during hardware emulation. The task is then executed in software in the RCC workstation (3107). When the software in the RCC system (3107) receives the testbench call signal (3101) from the behavior processor (3100, 3103), the behavior processor stops the hardware emulation while the RCC system (host workstation) processes the software task. After processing the task, the RCC system sends a signal back (3109b) to the behavior processor (3109) so that hardware emulation can resume. *See*, specification p. 204-206

**GROUNDS OF OBJECTION AND REJECTION TO BE REVIEWED ON APPEAL**

I. Claims 29 and 34 are objected to for containing unclear language.

II. Claims 1-11, 13-15, 17-30, 32-34, and 36 stand rejected under 35 U.S.C. 102 (b) as anticipated by U.S. Patent No. 5,838,948 issued to Bunza.

III. Claims 4, 16, 31 and 35 stand rejected under 35 U.S.C. 103(a) as obvious over U.S. Patent No. 5,838,948 issued to Bunza in view of IEEE Std 1364-1995 "IEEE Standard Hardware Description Languange Based on the Verilog Hardware Description Language".

IV. Claims 12 and 37 stand rejected under 35 U.S.C. 103(a) as obvious over U.S. Patent No. 5,838,948 issued to Bunza in view of IEEE article "A 145MHz User-Programmable Gate Array" by Eduardo do Valle Simoes et al.

**ARGUMENT**

**I. OBJECTION OF CLAIMS 29 and 34**

The Examiner has objected to claims 29 and 34 as containing limitations expressed in unclear language such that the Examiner considers claims 28 and 29 to be synonymous. The Appellants submit that the scope of claims 28 and 29 is significantly different and, therefore, cannot be considered synonymous. For example, in one embodiment of the invention, the testbench process is one of the processes that is executed by the host workstation. As recited in Claim 27, when a service request occurs a signal is sent to the testbench process in the host workstation. Claims 28 and 29 separately claim which component, "workstation" generally or "testbench process" specifically, will service the signal. The general use of the host workstation to service the signal (claim 28) is of significantly different scope than the recitation of using the specific testbench process to service the signal (claim 29). For example, claim 28 contemplates that the host workstation may suspend operation until the signal is serviced. Since the claim is silent regarding what specific process may service the signal, a process other than the testbench process may service the signal. In contrast, claim 29 specifically recites that the testbench process operates to service the signal. Thus, claim 29 is narrower in scope than claim 28. Since the scope of these claims is substantially different, claims 28 and 29 should not be considered synonymous.

The Examiner has similarly objected to claims 33 and 34. Claim 33 recites:

> The method of claim 32, further comprising step:
> suspending the operation of the simulation until the host workstation services the interrupt.
> (emphasis added)

Claim 34 recites:

> The method of claim 32, further comprising step:
> suspending the operation of the simulation until the testbench process services the interrupt.
> (emphasis added)

Claims 33 and 34 separately claim which component, "workstation" generally or "testbench process" specifically, will service the interrupt. The testbench process (3101) and host work station (RCC system) (3107) are different and distinct. Further, the specification clearly states on page 204: "the behavior processor provides a hardware-based "interrupt" -like control. When some condition (as defined by the user based on his

user design) is satisfied within the behavior processor, it sends a control signal back to the RCC system and any testbench processes." (emphasis added to the original) The Appellant notes that the specification clearly differentiates between the workstation of claim 33 and the testbench process of claim 34. Therefore, workstation and testbench process are not synonymous and the Examiner's objection is in error.

As such, in view of the argument herein and the previously filed response to the Final Office Action, the Appellants respectfully request that the objection to claims 29 and 34 be withdrawn.

**II. REJECTION OF CLAIMS 1-11, 13-15, 17-30, 32-34, and 36 under 35 U.S.C. 102 (b)**

The Examiner has rejected claims 1-11, 13-15, 17-30, 32-34, and 36 under 35 U.S.C. 102 (b) as anticipated by United States Patent No. 5,838,948 issued Nov. 17, 1998 to *Bunza* (hereinafter referred to as "*BU'948*"). The interpretation of *BU'948* by the Examiner is clearly erroneous. Simply stated, *BU'948* does not teach using a programmable logic element for modeling a portion of a design that includes a behavior function. In support of the rejection, the Examiner has cited a specific clause of *BU'948* and used the inherency doctrine for the basis of this rejection. The Appellants contend that this rejection is incorrect as a matter of law and fact. In addition, the Appellants submit that, even if, *arguendo*, the Examiner's basis for the rejection is correct, the reference does not contain an enabling disclosure regarding modeling a behavior function in a programmable logic element.

*BU'948* states, at column 9, lines 49-52, that the "use of unsynthesizable behavioral or high-level design representations, typical of early stages of design, are precluded by the use of hardware emulators." In the Final Office Action, at the top of page 4, the Examiner states that this quote teaches that "unsynthesizable" behavioral representations are precluded from being synthesized in a hardware emulator. The Appellants agree. The Examiner further states that this clause "does not teach that synthesizable behavioral representations of the design are precluded from being synthesized in hardware emulator." Further, the Examiner states that it is inherent from this teaching in *BU'948* that "behavioral or high level representations can be synthesized into hardware emulator". The Examiner is contending that the statement that "unsynthesizable" behavioral representations are not emulated in hardware, somehow

implies that synthesizable behavioral representations are able to be emulated in hardware. The Appellants believe that as a matter of law and fact, the Examiner can not conclude that hardware modeling of synthesizable behavioral representations are inherently disclosed from the BU'948 reference.

The mere fact that a certain result or characteristic *may* occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). Thus, "[t]o establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted); *see also*, *MPEP* §2112 IV. Because *BU'948* made a statement about "unsynthesizable" functions does not "necessarily and inevitably" teach that synthesizable behavioral functions can be modeled in hardware. As is well-known in the art (see *BU'948* at col. 5, lines 65-66), synthesizable behavioral functions may be modeled in software, i.e., a simulation. Consequently, the silence regarding synthesizable functions in *BU'948* does not necessarily and inevitably lead one skilled in the art to model such behavioral functions using a programmable logic element. Clearly, such functions could be modeled in software. Therefore, since the Examiner has agreed that *BU'948* states that unsynthesizable behavioral functions are not modeled in hardware and the above argument shows that synthesizable behavioral function modeling is not inherent from the statement in *BU'948*, the Appellants submit that *BU'948* does not teach modeling of behavioral functions in a programmable logic element. Thus, the rejection based upon BU'948 is improper and should be withdrawn.

The Examiner states in the Examiner's Advisory Action on page 2, "There is no support in the specification that teaches unsynthesizable behavioral level function can be

synthezied [sic] in the hardware emulator." The Appellants respectfully disagree with this contention and point out that the specification fully supports modeling of behavioral level functions by the emulator. Specifically, page 192 of Appellants' specification states:

> "One embodiment of the present invention provides a system that generates hardware elements from normally non-synthesizable code elements for placement on an FPGA device. This particular FPGA device is called a Behavior Processor. This Behavior Processor executes in hardware those code constructs that were previously executed in software."

Clearly, the Appellants specification teaches that the present invention models, in hardware, code elements that were previously non-synthesizable. *BU'948*, in contrast, teaches away from this particular embodiment of the invention stating "[u]se of unsynthesizable behavioral or high-level design representations, typical of early stages of design, are precluded by the use of hardware emulators." As such, the present invention comprises a particular embodiment that *BU'948* states is not possible.

Furthermore, *BU'948*, even if, *arguendo*, the modeling of synthesizable behavioral functions were inherent from the statement that unsynthesizable behavioral functions were precluded from hardware modeling, the teachings of *BU'948* do not show how one skilled in the art would model a behavior function in a programmable logic element. Since *BU'948* is silent regarding the specific nature and use of such functions in hardware, the Appellants submit that a teaching of an implementation can not be inherent from the statement that the "use of unsynthesizable behavioral or high-level design representations, typical of early stages of design, are precluded by the use of hardware emulators" (*BU'948*, col. 9, lines 49-52), i.e., *BU'948* is not enabling with regard to the Appellants invention.

> "The mere fact that a disclosure is contained in a patent or application and thus constructively reduced to practice, or that it is found in a printed publication, does not make the disclosure itself any more meaningful to those skilled in the art (and thus, ultimately, to the public). Rather, the criterion is whether the disclosure is sufficient to enable one skilled in the art to reduce the disclosed invention to practice. In other words, the disclosure must be such as will give possession of the invention to the person of ordinary skill. Even the act of publication or the fiction of constructive reduction to practice will not suffice if the disclosure does not meet this standard." In re Borst, 52 C.C.P.A. 1398, 345 F.2d 851, 854, 145 U.S.P.Q. (BNA) 554, 556 (CCPA 1965).

One skilled in the art could not be taught to create a hardware model of a behavioral function from silence. As such, the Appellants submit that the rejection based upon BU'948 is improper for this additional reason and the rejection should be withdrawn.

Appellants' claim 1 specifically recites a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavioral level function. "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added). Since, as argued above, *BU'948* lacks any disclosure of a behavior level function being modeled in a reprogrammable logic element nor a testbench call back process, the Appellants contend that claims 1-11, 13-15, 17-30, 32-34, and 36 are patentable over *BU'948* and, as such, fully satisfy the requirements of 35 U.S.C. §102 and are patentable thereunder.

Regarding Claims 2 and 3

Appellants' claim 2 recites that the behavior level function includes a condition. Appellants' claim 3 recites the occurrence of the condition triggers the testbench callback process. The Examiner cites *BU'948* col. 13, lines 55-64 as teaching a behavior level function includes a condition and col, 13, lines 17-23 as teaching the test bench call back process. As stated above, *BU'948* is devoid of any teaching of a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function, and thus devoid of a behavior level function that includes a condition. Further, even though the cited portions of BU'948 recite "a condition" and communication between a process emulator and a hardware simulator, the "condition" is not part of a behavior level function as claimed by the Appellants. Since *BU'948* does not teach a behavior level function having a condition, *BU'948* cannot teach the condition triggers the testbench callback process. Therefore, *BU'948* does not anticipate claims 2 and 3 under 35 U.S.C. §102 and claims 2 and 3 are patentable thereunder.

Regarding Claims 5 and 6

Appellants' claim 5 recites that the signal includes an interrupt from the testbench call back process to the host testbench process. Appellants' claim 6 recites the signal includes an interrupt from the reprogrammable logic element to the host testbench process. The Examiner cites *BU'948* col. 13, lines 8-36; 60-64 as teaching the elements of claims 5 and 6. As stated above, *BU'948* is devoid of any teaching of a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function. Further, *BU'948* is devoid of any teaching the signal includes an interrupt from the testbench call back process to the host testbench process and devoid of any teaching the signal includes an interrupt from the reprogrammable logic element to the host testbench process. In contrast, *BU'948* teaches control circuitry and a control program identifies conditions which require communication between the process emulator and hardware simulator such as interrupt handling. However, there is no teaching of interrupting "the host testbench process". Since at least one element of claims 5 and 6 is not present in *BU'948*, *BU'948* does not anticipate claims 5 and 6. Therefore, *BU'948* does not anticipate claims 5 and 6 under 35 U.S.C. §102 and claims 5 and 6 are patentable thereunder.

Regarding Claim 7

Appellants' claim 7 recites that the signal includes data from the testbench call back process to the host testbench process. Claim 7 depends directly from independent claim 1. As stated above, *BU'948* is devoid of any teaching of a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function. The Examiner cites *BU'948*, col. 12, lines 25-32, 4-6 as teaching the elements of claim 7. In contrast, the cited portion does not teach the testbench call back process to the host testbench process. The cited portion teaches a "mapper" and a "translator" that work together to allow data to be communicated between a processor emulator and a hardware simulator. There is no teaching of data flowing between two processes, i.e., the testbench callback process and the host testbench process. Further, *BU'948* is devoid of any teaching the signal includes data from the testbench call back process to the host testbench process. Therefore, *BU'948* does not anticipate claim 7 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 8

Appellants' claim 8 recites a reprogrammable logic element temporarily suspends operation upon the occurrence of the condition. Claim 8 depends indirectly from independent claim 1. The Examiner cites *BU'948* col. 15, lines 8-13 as teaching all the elements of claim 8. The portion cited by the Examiner is totally devoid of a reprogrammable logic element temporarily suspending operation. As stated above, *BU'948* is devoid of any teaching of a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavioral level function. Further, *BU'948* is devoid of any teaching a reprogrammable logic element temporarily suspends operation upon the occurrence of the condition. Therefore, *BU'948* does not anticipate claim 8 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 9

Appellants' claim 9 recites that the reprogrammable logic element resumes operation from the point at which operation was temporarily suspended upon the service of the signal by the host testbench process. Claim 9 depends indirectly from independent claim 1. The Examiner cites *BU'948* col. 15, lines 8-35 as teaching the elements of claim 9. In contrast, the cited portion teaches "the system in step 332, completes the hardware simulation cycles 206 in the manner described above. When the simulator 206 has completed the required cycles, the system 200 moves to step 334, and resumes normal execution of the target program 22. The hardware simulator described by *BU'948* is software and not a reprogrammable logic element (hardware). Further, there is no mention of a reprogrammable logic element resuming a suspended operation from the point at which the operation was temporarily suspended upon service of the signal in the section cited by the Examiner. As stated above, *BU'948* is devoid of any teaching of a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function. Further, *BU'948* is devoid of any teaching the reprogrammable logic element resumes operation from the point at which operation was temporarily suspended upon the service of the signal by the host testbench process.

Therefore, *BU'948* does not anticipate claim 9 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 10

Appellants' claim 10 recites the reprogrammable logic element temporarily pauses operation upon the occurrence of the condition. The Examiner cites *BU'948* col. 7, lines 63-67; col. 15, lines 8-13 as teaching all the elements of claim 10. Column 7, lines 63 to 67 teaches the "physical microprocessors must wait for the each simulation cycle to be completed by the hardware simulator". Assuming this waiting is interpreted as pausing, it is the physical microprocessor that pauses and not the reprogrammable logic element. *BU'948* defines the physical microprocessor as a conventional processor emulator typically available from Applied Microsystems Corporation. *See, BU'948* col. 8, lines 18-22. The processor of *BU'948* is clearly different from the reprogrammable hardware emulator of the present invention. Further, the pause referenced in this section is not in response to the occurrence of the "condition". Column 15, lines 8-13 as discussed above, refers only to the hardware simulator (software) disclosed by *BU'948* and not to a reprogrammable logic element. For these and other reasons, the cited portions of *BU'948* simply do not teach all the elements of claim 10. Claim 10 depends indirectly from independent claim 1. As stated above, *BU'948* is devoid of any teaching of a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavioral level function. Further, *BU'948* is devoid of any teaching the reprogrammable logic element temporarily pauses operation upon the occurrence of the condition. Therefore, *BU'948* does not anticipate claim 10 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 11

Appellants' claim 11 recites the reprogrammable logic element includes a clock that controls the speed of processing instructions and data in the reprogrammable logic element. The Examiner cites col. 7, lines 61-67 as teaching all the elements of claim 11. The cited portion teaches the processor in a hardware modeler is often a dynamic device that must maintain a running clock in order to retain data. However, the cited portion

does not teach the processor is a reprogrammable logic element. Nor can it be inferred that the processor is a reprogrammable logic element. *BU'948* defines the physical microprocessor as a conventional processor emulator typically available from Applied Microsystems Corporation. *See*, *BU'948* col. 8, lines 18-22. The processor of *BU'948* is clearly different from the reprogrammable hardware emulator of the present invention. Claim 11 depends directly from independent claim 1. As stated above, *BU'948* is devoid of any teaching of a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function. Further, *BU'948* is devoid of any teaching the reprogrammable logic element includes a clock that controls the speed of processing instructions and data in the reprogrammable logic element. Therefore, *BU'948* does not anticipate claim 11 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 13

Appellants' claim 13 recites a behavior processor for modeling a second hardware model of a selected portion of the user design. The behavior processor models "behavior functions" in a hardware model of a selected portion of the user design. As discussed above, *BU'948* states, at column 9, lines 49-52, that the "use of unsynthesizable behavioral or high-level design representations, typical of early stages of design, are precluded by the use of hardware emulators." In the Final Office Action, at the top of page 4, the Examiner states that this quote teaches that "unsynthesizable" behavioral representations are precluded from being synthesized in a hardware emulator. The Examiner has conceded *BU'948* does not teach a "behavior processor" for modeling "behavior functions" in a hardware model of a selected portion of the user design; In contrast, *BU'948* teaches behavioral representations are precluded from being synthesized in a hardware emulator and Appellants respectfully agree.

The Examiner cites *BU'948*, column 13, lines 55-60 as teaching a behavioral processor as a software kernel, control program and associate control circuitry surrounding the hardware emulator. The portion cited by the Examiner simply does not teach a behavior processor. Instead, the portion cited teaches certain conditions require the processor emulator (hardware) to communicate with hardware simulator (software)

such as explicit memory references outside of the loaded target program address range, input/output operations, interrupt handling, and instructions dealing with explicit hardware functions. There is simply no teaching of using a behavior processor to model behavior functions in hardware in the cited section, nor anywhere throughout the rest of *BU'948.* Therefore, *BU'948* does not anticipate claim 13 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 14

Appellants' claim 14 recites that the selected portion includes a behavioral aspect of the user design. The Examiner cites *BU'948* col. 5, lines 62-67 and col. 6,lines 10-13 as teaching modeling a hardware model for a portion of the user design that includes behavioral aspects of the user design. Claim 14 depends directly from claim 13. As discussed above, *BU'948* does not disclose a "behavior processor". For this reason and the reasons discussed above with regard to claims 1 and 13, *BU'948* does not teach each and every element of claim 14. Therefore, *BU'948* does not anticipate claim 14 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 15

Appellants' claim 15 recites that the selected portion includes at least one condition in the user design. The Examiner has rejected claim 15 for the same reasons as claim 2. Claim 15 depends directly from claim 13. As discussed above, claim 13 requires a "behavior processor". *BU'948* is totally devoid of any teaching of a behavior level processor. For this reason and the reasons discussed above with regard to claims 1, 2 and 13, *BU'948* does not teach each and every element of claim 15. Therefore *BU'948* cannot anticipate claim 15 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 17

Appellants' claim 17 recites that the behavior processor includes a testbench callback process for responding to the selected portion of the user design modeled in the reprogrammable hardware emulator by sending a signal to the host workstation. The Examiner has rejected claim 17 for the same reasons as claim 1. Claim 17 depends from

claim 13. As discussed above, claim 13 requires a "behavior processor". *BU'948* is totally devoid of any teaching of a behavior level processor. For this reason and the reasons discussed above with regard to claims 1 and 13, *BU'948* does not teach each and every element of claim 17. Therefore, *BU'948* does not anticipate claim 17 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 18

Appellants' claim 18 recites that the selected portion includes at least one condition in the user design and the behavior processor includes a testbench callback process for responding to the at least one occurrence of the condition in the reprogrammable hardware emulator by sending a signal to the host workstation. The Examiner has rejected claim 18 for the same reasons as claim 3. Claim 18 depends directly from claim 13. As discussed above, claim 13 requires a "behavior processor". *BU'948* is totally devoid of any teaching of a behavior level processor. For this reason and the reasons discussed above with regard to claims 1, 3 and 13, *BU'948* does not teach each and every element of claim 18. Therefore, *BU'948* does not anticipate claim 18 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 19

Appellants' claim 19 recites that the reprogrammable hardware emulator temporarily suspends operation upon the occurrence of the condition. The Examiner has rejected claim 19 for the same reasons as claim 8. Claim 19 depends indirectly from claim 13. As discussed above, claim 13 requires a "behavior processor". *BU'948* is totally devoid of any teaching of a behavior level processor. For this reason and the reasons discussed above with regard to claims 1, 8 and 13, *BU'948* does not teach each and every element of claim 19. Therefore, *BU'948* does not anticipate claim 19 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 20

Appellants' claim 20 recites the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended upon the service

of the signal by the host workstation. The Examiner has rejected claim 20 for the same reasons as claim 9. Claim 20 depends indirectly from claim 13. As discussed above, claim 13 requires a "behavior processor". *BU'948* is totally devoid of any teaching of a behavior level processor. For this reason and the reasons discussed above with regard to claims 1, 9 and 13, *BU'948* does not teach each and every element of claim 20. Therefore, *BU'948* does not anticipate claim 20 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 21

Appellants' claim 21 recites that the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended upon the service of the signal by the host workstation. The Examiner has rejected claim 21 for the same reasons as claim 10. Claim 21 depends indirectly from claim 13. As discussed above, claim 13 requires a "behavior processor". *BU'948* is totally devoid of any teaching of a behavior level processor. For this reason and the reasons discussed above with regard to claims 1, 10 and 13, *BU'948* does not teach each and every element of claim 21. Therefore, *BU'948* does not anticipate claim 21 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 22

Appellants' claim 22 recites that the selected portion includes at least one condition for the user design and the behavior processor sends a wait signal to the reprogrammable hardware emulator upon the at least one occurrence of the condition so that the reprogrammable hardware emulator temporarily suspends operation. The Examiner has rejected claim 22 for the same reasons as claim 8. Further, the Examiner cites *BU'948*, col. 7, lines 63-67 as teaching the wait is executed by the reprogrammable logic element on occurrence of a condition. The portion of *BU'948* cited by the Examiner does not teach the reprogrammable hardware emulator temporarily suspends operation. The cited portion discloses the physical microprocessor in the hardware modeler must wait for each simulation cycle to be completed by the hardware simulator. *BU'948* defines the physical microprocessor as a conventional processor emulator typically

available from Applied Microsystems Corporation. *See, BU'948* col. 8, lines 18-22. The processor of *BU'948* is clearly different from the reprogrammable hardware emulator of the present invention. Claim 22 depends directly from claim 13. As discussed above, claim 13 requires a "behavior processor". *BU'948* is totally devoid of any teaching of a behavior level processor. For this reason and the reasons discussed above with regard to claims 1, 8 and 13, *BU'948* does not teach each and every element of claim 22. Therefore, *BU'948* does not anticipate claim 22 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 23

Appellants' claim 23 recites that the behavior processor sends a resume signal to the reprogrammable hardware emulator upon the service of the signal by the host workstation so that the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended. The Examiner has rejected claim 23 for the same reasons as claim 9. Claim 23 depends indirectly from claim 13. As discussed above, claim 13 requires a "behavior processor". *BU'948* is totally devoid of any teaching of a behavior level processor. For this reason and the reasons discussed above with regard to claims 1, 9 and 13, *BU'948* does not teach each and every element of claim 23. Therefore, *BU'948* does not anticipate claim 23 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 24

Appellants' claim 24 recites that the behavior processor toggles the wait signal to the reprogrammable hardware emulator upon the service of the signal by the host workstation so that the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended. The Examiner has rejected claim 23 for the same reasons as claim 10. Claim 24 depends indirectly from claim 13. As discussed above, claim 13 requires a "behavior processor". *BU'948* is totally devoid of any teaching of a behavior level processor. For this reason and the reasons discussed above with regard to claims 1, 10 and 13, *BU'948* does not teach each and every element

of claim 24. Therefore, *BU'948* does not anticipate claim 24 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 25

Appellants' claim 25 recites that the behavior processor operates when it receives a request for service from the host workstation. The Examiner cites *BU'948* col. 12, lines 19-26 as teaching all the elements of claim 25. The portion of *BU'948* cited by the Examiner discloses how the processor emulator (hardware) communicates with the hardware simulator (software) via a mapper and a translator. The cited portion of *BU'948*, and *BU'948* in its entirety, does not disclose a behavior processor. Thus, there is no disclosure by *BU'948* of how the behavior processor operates when it receives a request for service from the host workstation. Claim 25 depends directly from claim 13. As discussed above, claim 13 requires a "behavior processor". *BU'948* is totally devoid of any teaching of a behavior level processor. For this reason and the reasons discussed above with regard to claims 1 and 13, *BU'948* does not teach each and every element of claim 25. Therefore, *BU'948* does not anticipate claim 25 under 35 U.S.C. §102 and is patentable.

Regarding Claim 26

Appellants' claim 26 recites that the behavior processor operates when it receives a request for service from the reprogrammable hardware emulator. The Examiner cites *BU'948* col. 12, lines 4-19 as teaching all the elements of claim 26. The portion of *BU'948* cited by the Examiner discloses how the processor emulator (hardware) communicates with the hardware simulator (software) via a mapper and a translator. The cited portion of *BU'948*, and *BU'948* in its entirety, does not disclose a behavior processor. Thus, there is no disclosure by *BU'948* of how the behavior processor operates when it receives a request for service from the reprogrammable hardware emulator. Claim 26 depends directly from claim 13. As discussed above, claim 13 requires a "behavior processor". *BU'948* is totally devoid of any teaching of a behavior level processor. For this reason and the reasons discussed above with regard to claims 1 and 13, *BU'948* does not teach

each and every element of claim 26. Therefore, *BU'948* does not anticipate claim 26 under 35 U.S.C. §102 and is patentable.

Regarding Claim 27

The Examiner has rejected claim 27 for the same reasons as claim 1. Claim 27 specifically recites:

> A method of verifying a user design where the verification environment includes a host workstation for running a simulation of the user design and a testbench process, comprising steps:
> modeling a behavioral portion of the user design in hardware, where the behavioral portion includes a service request; and
> sending a signal to the testbench process in the host workstation upon the occurrence of the service request. (emphasis added)

As discussed above in regard to claim 1, *BU'948* teaches away from modeling a behavioral portion of the user design in hardware. *BU'948* states, at column 9, lines 49-52, that the "use of unsynthesizable behavioral or high-level design representations, typical of early stages of design, are precluded by the use of hardware emulators." Further, *BU'948* does not disclose how one skilled in the art could model a behavioral portion of the user design in hardware. As such, the Appellants submit that the rejection based upon *BU'948* is improper for this additional reason. For these reasons, and the arguments presented above in regard to claim 1, the Appellants respectfully request that the rejection to claim 27 be withdrawn.

Regarding Claim 28

Appellants' claim 28 recites suspending the operation of the simulation until the host workstation services the signal. The Examiner has rejected claim 28 for the same reasons as claim 9. Claim 28 depends directly from claim 27. As discussed above, claim 27 discloses modeling a behavioral portion of the user design in hardware. *BU'948* is totally devoid of any teaching of modeling a behavioral portion of the user design in hardware. For this reason and the reasons discussed above with regard to claims 1, 9 and 27, *BU'948* does not teach each and every element of claim 28. Therefore, *BU'948* does not anticipate claim 28 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 29

Appellants' claim 29 recites suspending the operation of the simulation until the testbench process services the signal. The Examiner cites *BU'948*, col. 15, lines 8-13 as teaching all the elements of claim 28. The portion of *BU'948* does not teach suspending the operation of the simulation until the testbench process services the signal. In contrast, the cited portion teaches certain processor interface functions require a response from the target circuitry, while other processor interface functions do not require a response from the target circuitry. Claim 29 depends directly from claim 27. As discussed above, claim 27 discloses modeling a behavioral portion of the user design in hardware. *BU'948* is totally devoid of any teaching of modeling a behavioral portion of the user design in hardware. For this reason and the reasons discussed above with regard to claims 1 and 27, *BU'948* does not teach each and every element of claim 29. Therefore, *BU'948* does not anticipate claim 28 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 30

Appellants' claim 28 recites the step of modeling the behavioral portion includes modeling conditional statements. The Examiner has rejected claim 30 for the same reasons as claim 2. Claim 30 depends directly from claim 27. As discussed above, claim 27 discloses modeling a behavioral portion of the user design in hardware. *BU'948* is totally devoid of any teaching of modeling a behavioral portion of the user design in hardware. For this reason and the reasons discussed above with regard to claims 1, 2 and 27, *BU'948* does not teach each and every element of claim 30. Therefore, *BU'948* does not anticipate claim 30 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 32

The Examiner has rejected claim 32 for the same reasons as claim 1. Appellants' claim 32 recites:

> A method of verifying a user design where the verification environment includes a host workstation for running a simulation of the user design and a testbench process, comprising steps:

> modeling a conditional portion of the user design in a hardware environment;
> executing the conditional portion in the hardware environment; and
> sending an interrupt to the testbench process in the host upon the occurrence of at least one condition in the conditional portion. (emphasis added)

The Examiner further cites *BU'948* col. 13, lines 8-36; 60-64 as teaching the sending of an interrupt from the test bench call back process to the host/test bench process as an I/O trap initiated by the reprogrammable logic element (process emulator). As discussed above, the process emulator disclosed *BU'948* is not the same as the reprogrammable logic element. *BU'948* defines the physical microprocessor as a conventional processor emulator typically available from Applied Microsystems Corporation. *See*, *BU'948* col. 8, lines 18-22. Further *BU'948* is devoid of any teaching of modeling a conditional portion of the user design in a hardware environment. For these reasons, and the arguments presented above in regard to claim 1, the Appellants request the rejection to claim 32 be withdrawn.

Regarding Claim 33

Appellants' claim 33 recites suspending the operation of the simulation until the host workstation services the interrupt. The Examiner has rejected claim 33 for the same reasons as claim 9. Claim 33 depends directly from claim 32. As discussed above, claim 32 discloses modeling a conditional portion of the user design in a hardware environment. *BU'948* is totally devoid of any teaching of modeling a conditional portion of the user design in a hardware environment. For this reason and the reasons discussed above with regard to claims 1, 9 and 32, *BU'948* does not teach each and every element of claim 33. Therefore, *BU'948* does not anticipate claim 33 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 34

Appellants' claim 34 recites suspending the operation of the simulation until the testbench process services the interrupt. The Examiner cites *BU'948* col. 15, lines 8-13 as teaching all the elements of claim 34. The portion of *BU'948* does not teach

suspending the operation of the simulation until the testbench process services the interrupt. In contrast, the cited portion teaches certain processor interface functions require a response from the target circuitry, while other processor interface functions do not require a response from the target circuitry. Claim 34 depends directly from claim 32. As discussed above, claim 32 discloses modeling a behavioral portion of the user design in hardware. *BU'948* is totally devoid of any teaching of modeling a behavioral portion of the user design in hardware. For this reason and the reasons discussed above with regard to claims 1 and 32, *BU'948* does not teach each and every element of claim 34. Therefore, *BU'948* does not anticipate claim 34 under 35 U.S.C. §102 and is patentable thereunder.

Regarding Claim 36

Appellants' claim 36 recites that the step of executing occurs at the speed of a hardware clock. The Examiner has rejected claim 36 for the same reasons as claim 11. The Examiner cites col. 7, lines 61-67 as teaching all the elements of claim 36. The cited portion teaches the processor in a hardware modeler is often a dynamic device that must maintain a running clock in order to retain data. However, the cited portion does not teach the processor is a reprogrammable logic element. Nor can it be inferred that the processor is a reprogrammable logic element. *BU'948* defines the physical microprocessor as a conventional processor emulator typically available from Applied Microsystems Corporation. *See*, *BU'948* col. 8, lines 18-22. The processor of *BU'948* is clearly different from the reprogrammable hardware emulator of the present invention. Claim 36 depends directly from independent claim 32. As discussed above, claim 32 discloses modeling a behavioral portion of the user design in hardware. *BU'948* is totally devoid of any teaching of modeling a behavioral portion of the user design in hardware. For this reason and the reasons discussed above with regard to claims 1 and 32, *BU'948* does not teach each and every element of claim 36. Therefore, *BU'948* does not anticipate claim 36 under 35 U.S.C. §102 and is patentable thereunder.

**III. REJECTION OF CLAIMS 4, 16, 31, and 35 under 35 U.S.C. 103(a)**

The Examiner has rejected claims 4, 16, 31 and 35 in the present application under 35 U.S.C. 103(a). The rejections are based upon various combinations of IEEE 1364 with *BU'948*. As discussed above, *BU'948* does not anticipate the Appellants' present invention. The Examiner concedes that IEEE 1364 does not anticipate any of the independent claims, claims 1, 13, 27,and 32, currently pending in the application. As discussed in further detail below, IEEE 1364, singly or in combination, with *BU'948* does not render Appellants' invention obvious under 35 U.S.C. 103(a).

Regarding Claims 4, 16, 31 and 35

The Examiner has grouped together dependent claims 4, 16, 31 and 35 and rejected them under 35 U.S.C. 103(a) as being unpatentable over *BU'948 in view of* IEEE1364.

Independent claims 1, 13, 27, and 32, as discussed above, recite a reprogrammable logic element that models a behavior function (or behavioral portion) of a user design. *BU'948* does not teach or suggest modeling a behavior function or behavioral portion of a user design in a reprogrammable logic element nor does BU'948 teach the use of a testbench call back process.

IEEE1364 teaches conditional expression for state dependent paths, but is devoid of any teaching or suggestion of using a reprogrammable logic element to model a behavioral function of a user design. Nor is there any disclosure of using a testbench call back process that responds to the behavioral function. Since the same elements are lacking from both *BU'948* and IEEE1364, no permissible combination of these references teaches or suggests the applicants' invention as recited in independent claims, 1, 13, 27, and 32.

Claims 4, 16, 31, and 35 depend, either directly or indirectly, from claims 1, 13, 27, and 32 and recite additional features therefor. Since a combination of *BU'948* and IEEE1364 would not produce applicants' invention as recited in claims 1, 13, 27, and 32, dependent claims 4, 16, 31, and 35 are also not obvious and are allowable.
Thus, the applicants submit that claims 4, 16, 31, and 35 are patentable over BU'948 in view of IEEE1364. Accordingly, the applicants respectfully request the rejection be withdrawn.

Regarding Claims 12 and 37

The Examiner has rejected claims 12 and 37 as unpatentable under 35 U.S.C. 103(a) as being unpatentable over *BU'948* in view of ED1995.

Independent claims 1 and 32, as discussed above, recite a reprogrammable logic element that models a behavior function or behavioral portion of a user design. *BU'948* does not teach or suggest modeling a behavioral function or portion in a reprogrammable logic element nor does *BU'948* teach a testbench call back process.

ED1995 teaches conditional expression for state dependent paths, but is devoid of any teaching or suggestion of using a reprogrammable logic element to model a behavioral function of a user design. Nor is there any disclosure of using a testbench call back process that responds to the behavioral function. Since the same elements are lacking from both *BU'948* and ED1995, no permissible combination of these references teaches or suggests the applicants' invention as recited in independent claims 1 and 32. Claims 12 and 37 depend, either directly or indirectly, from claims 1 and 32 and recite additional features therefor. Since the combination of *BU'948* and ED1995 would not produce Applicants' invention as recited in claims 1 and 32, dependent claims 12 and 37 are also not obvious and are allowable.

Thus, the applicants submit that claims 12 and 37 are patentable over *BU'948* in view of ED1995. Accordingly, the applicants respectfully request the rejection be withdrawn.

## CONCLUSION

For the reasons advanced above, Appellants respectfully urge that the rejections and objections of claims 1-37 are improper. Reversal of the rejections and objections in this appeal is respectfully requested.

Respectfully submitted,

5-17-06
Date

Raymond R. Moser Jr.
Registration No. 34,682

MOSER IP LAW GROUP
1040 Broad Street, 2nd Floor
Shrewsbury, NJ 07702

## CLAIMS APPENDIX

1. (Original) A behavior processor system for operating a portion of a user design and interfacing with a host testbench process, comprising:

a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function; and

a testbench call back process for responding to the behavior level function in the reprogrammable logic element by sending a signal to the host testbench process.

2. (Original) The system of claim 1, wherein the behavior level function includes a condition.

3. (Previously Presented The system of claim 2, wherein the behavior level function includes a condition and the occurrence of the condition triggers the testbench call back process.

4. (Original) The system of claim 2, wherein the condition includes an "if-then" conditional statement implemented in hardware.

5. (Original) The system of claim 1, wherein the signal includes an interrupt from the testbench call back process to the host testbench process.

6. (Original) The system of claim 1, wherein the signal includes an interrupt from the reprogrammable logic element to the host testbench process.

7. (Original) The system of claim 1, wherein the signal includes data from the testbench call back process to the host testbench process.

8. (Previously Presented) The system of claim 1, wherein a reprogrammable logic element temporarily suspends operation upon the occurrence of the condition.

9. (Original) The system of claim 8, wherein the reprogrammable logic element resumes operation from the point at which operation was temporarily suspended upon the service of the signal by the host testbench process.

10. (Original) The system of claim 2, wherein the reprogrammable logic element temporarily pauses operation upon the occurrence of the condition.

11. (Original) The system of claim 1, wherein the reprogrammable logic element includes a clock that controls the speed of processing instructions and data in the reprogrammable logic element.

12. (Original) The system of claim 11, wherein the clock runs at 20 MHz.

13. (Original) A verification system for analyzing a user design, comprising:

a host workstation for modeling and operating a software model of the user design;

a reprogrammable hardware emulator for modeling a first hardware model of at least a portion of the user design; and

a behavior processor for modeling a second hardware model of a selected portion of the user design.

14. (Original) The verification system of claim 13, wherein the selected portion includes a behavioral aspect of the user design.

15. (Original) The verification system of claim 13, wherein the selected portion includes at least one condition in the user design.

16. (Original) The verification system of claim 15, wherein the at least one condition includes an "if- then" conditional statement.

17. (Original) The verification system of claim 13, wherein the behavior processor includes a testbench callback process for responding to the selected portion of the user

design modeled in the reprogrammable hardware emulator by sending a signal to the host workstation.

18. (Previously Presented) The verification system of claim 13, wherein the selected portion includes at least one condition in the user design and the behavior processor includes a testbench callback process for responding to the at least one occurrence of the condition in the reprogrammable hardware emulator by sending a signal to the host workstation.

19. (Original) The verification system of claim 18, wherein the reprogrammable hardware emulator temporarily suspends operation upon the occurrence of the condition.

20. (Original) The verification system of claim 19, wherein the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended upon the service of the signal by the host workstation.

21. (Original) The verification system of claim 18, wherein the reprogrammable hardware emulator temporarily pauses operation upon the occurrence of the condition.

22. (Previously Presented) The verification system of claim 13, wherein the selected portion includes at least one condition for the user design and the behavior processor sends a wait signal to the reprogrammable hardware emulator upon the at least one occurrence of the condition so that the reprogrammable hardware emulator temporarily suspends operation.

23. (Original) The verification system of claim 22, wherein the behavior processor sends a resume signal to the reprogrammable hardware emulator upon the service of the signal by the host workstation so that the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended.

24. (Original) The verification system of claim 22, wherein the behavior processor toggles the wait signal to the reprogrammable hardware emulator upon the service of the signal by the host workstation so that the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended.

25. (Original) The verification system of claim 13, wherein the behavior processor operates when it receives a request for service from the host workstation.

26. (Original) The verification system of claim 13, wherein the behavior processor operates when it receives a request for service from the reprogrammable hardware emulator.

27. (Previously Presented) A method of verifying a user design where the verification environment includes a host workstation for running a simulation of the user design and a testbench process, comprising steps:

modeling a behavioral portion of the user design in hardware, where the behavioral portion includes a service request; and

sending a signal to the testbench process in the host workstation upon the occurrence of the service request.

28. (Original) The method of claim 27, further comprising step:
suspending the operation of the simulation until the host workstation services the signal.

29. (Original) The method of claim 27, further comprising step:
suspending the operation of the simulation until the testbench process services the signal.

30. (Original) The method of claim 27, wherein the step of modeling the behavioral portion includes modeling conditional statements.

31. (Previously Presented) The method of claim 30, wherein the step of modeling the conditional statements includes "if-then" statements.

32. (Original) A method of verifying a user design where the verification environment includes a host workstation for running a simulation of the user design and a testbench process, comprising steps:

modeling a conditional portion of the user design in a hardware environment;

executing the conditional portion in the hardware environment; and

sending an interrupt to the testbench process in the host upon the occurrence of at least one condition in the conditional portion.

33. (Original) The method of claim 32, further comprising step:
suspending the operation of the simulation until the host workstation services the interrupt.

34. (Original) The method of claim 32, further comprising step:
suspending the operation of the simulation until the testbench process services the interrupt.

35. (Previously Presented) The method of claim 32, wherein the step of modeling the conditional portion includes "if-then" statements.

36. (Original) The method of claim 32, wherein the step of executing occurs at the speed of a hardware clock.

37. (Original) The method of claim 36, wherein the step of executing occurs at 20 MHz.

## EVIDENCE APPENDIX

[None]

## RELATED PROCEEDINGS APPENDIX

[None]